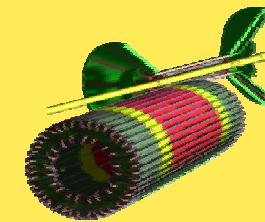


The ALICE Pixel Detector

P. Riedler, CERN
ALICE SPD Team

Overview

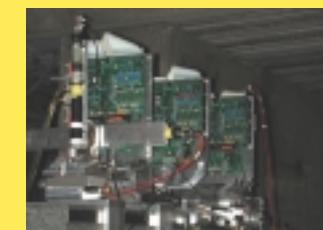
- *ALICE SPD*
 - Overview
 - Physics performance
 - Test Setups



- *ALICE1LHCb chip*
 - Single chip tests
 - Bus tests
 - Wafer probing



- *Assemblies and Ladders*
 - Source tests
 - Test beam



- *Conclusions and Summary*

Talks related to the ALICE SPD at this conference:

D.Barberis - Monday 9, 14:30-15:00

"Physics with second generation pixel detectors"

A.Kluge - Monday 9, 15:00-15:20

"The read out system of the ALICE pixel detector"

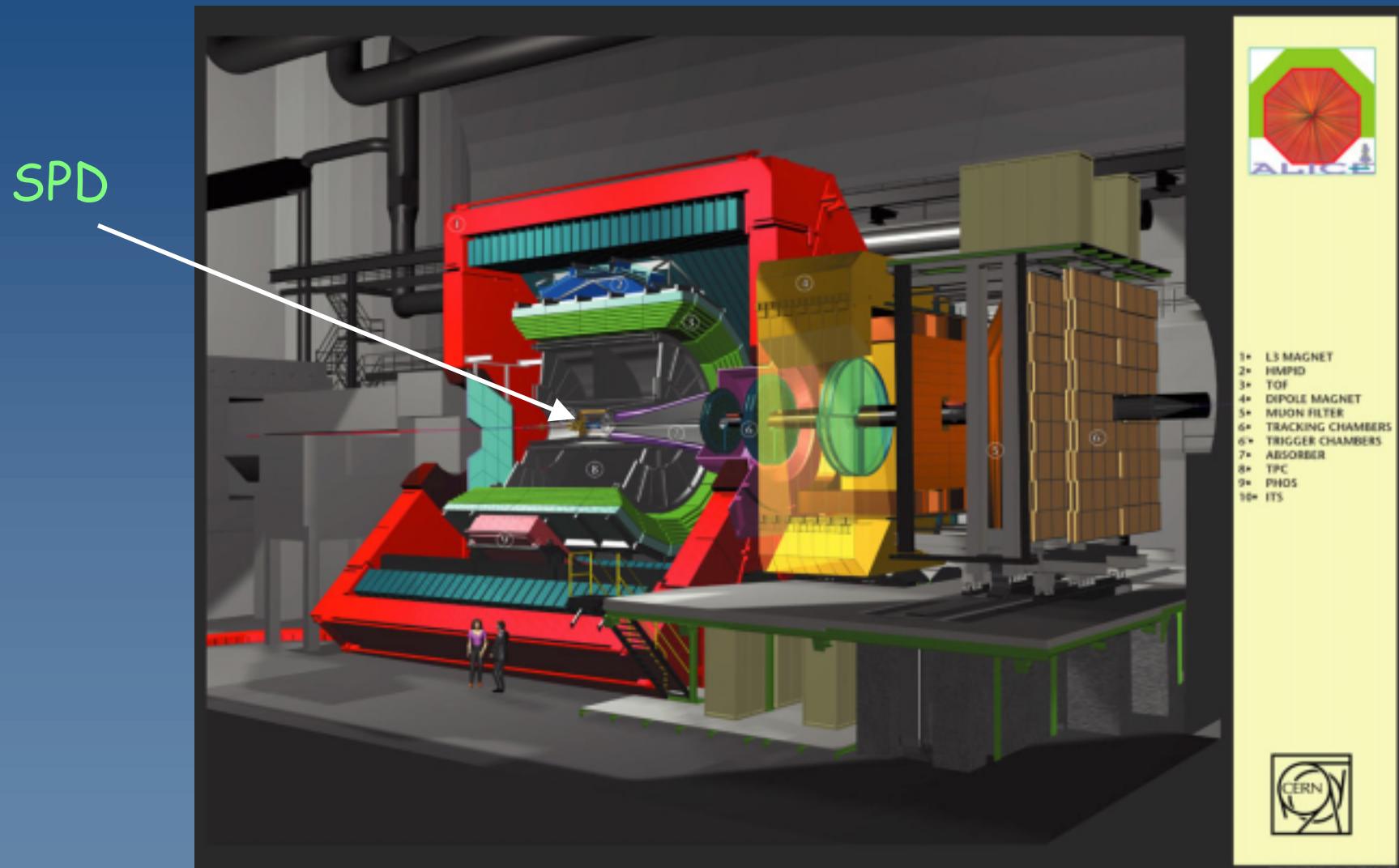
K.Wyllie - Monday 9, 15:20-15:40

"Front-end pixel chips for Tracking in ALICE and particle identification in LHCb"

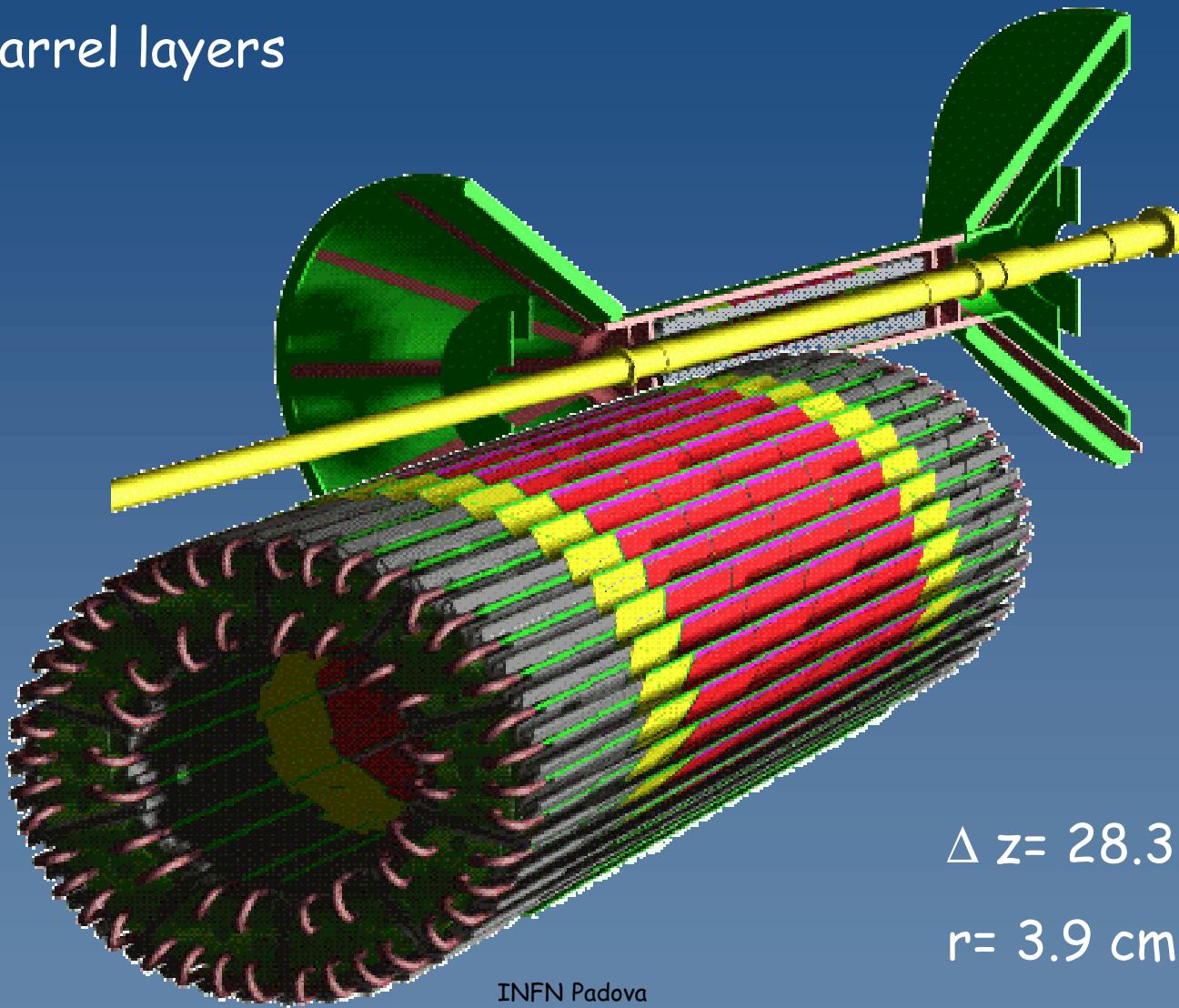
J.Salonen - Thursday 12, 9:20-9:40

"Flip Chip Hybridization of Pixel Detectors for ALICE and LHCb Experiments "

ALICE Silicon Pixel Detector - Overview



2 barrel layers

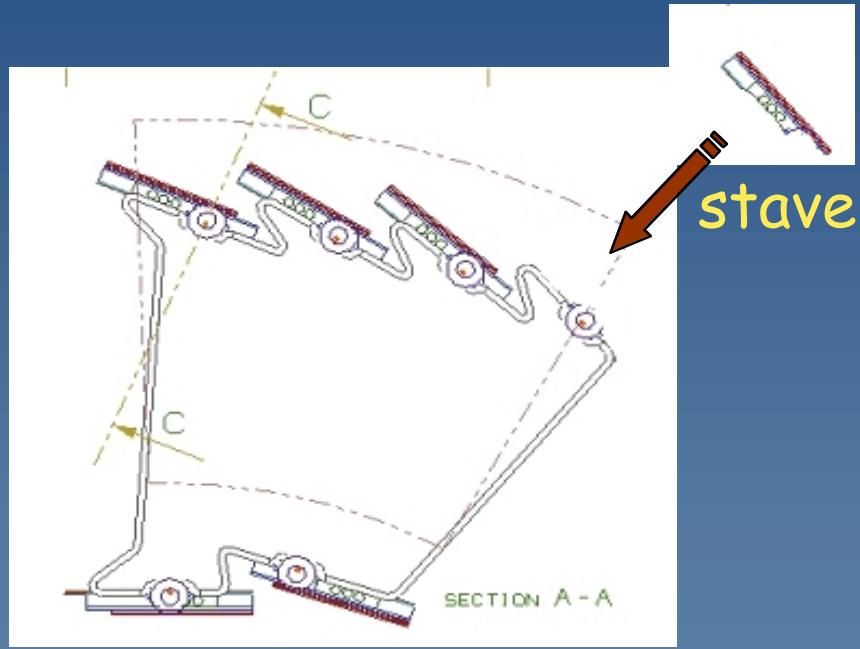


$\Delta z = 28.3 \text{ cm}$

$r = 3.9 \text{ cm} \& 7.6 \text{ cm}$

INFN Padova

The two barrels will be built of 10 sectors, each equipped with 6 staves:



INFN Padova

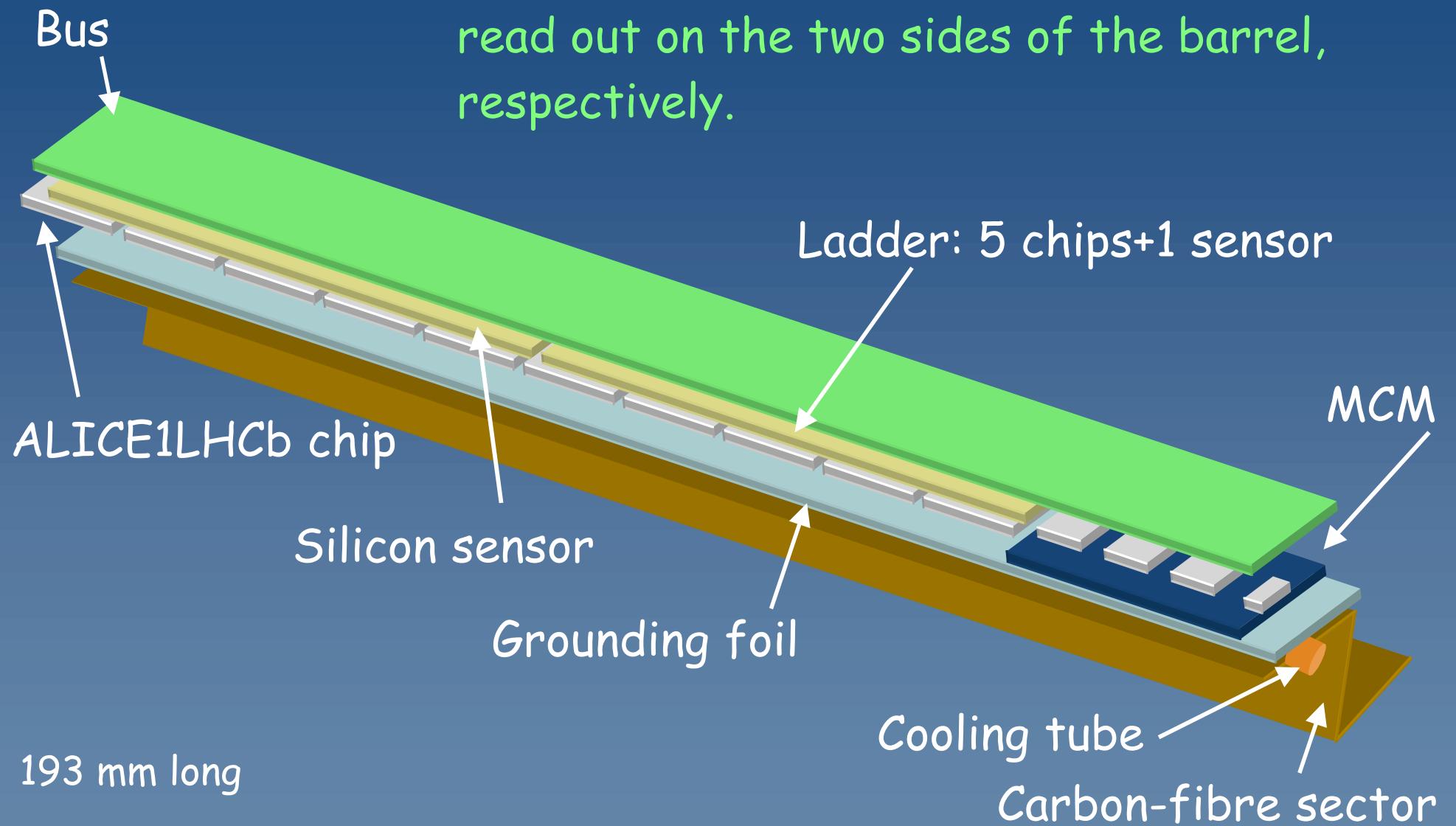
Sector - Carbon Fibre Support



INFN Padova

Material budget(each layer)

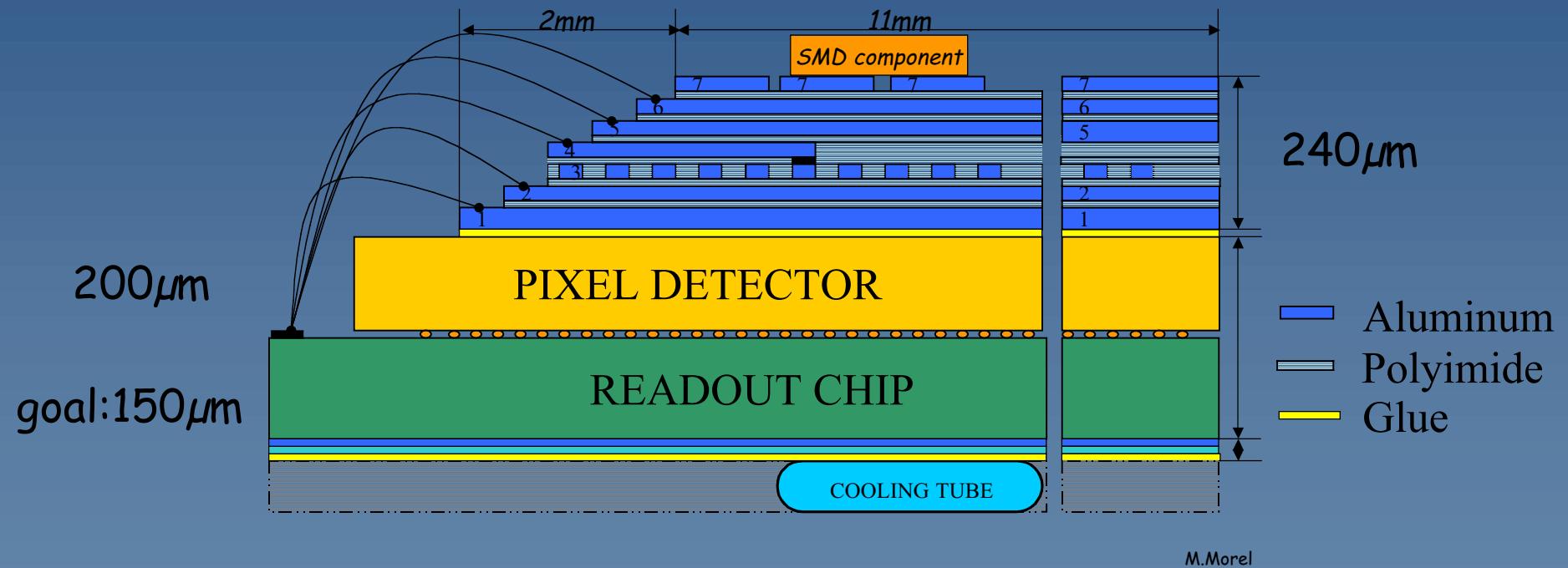
$\approx 0.9\% X_0$ ($Si \approx 0.37$, cooling ≈ 0.3 , bus 0.17, support ≈ 0.1)



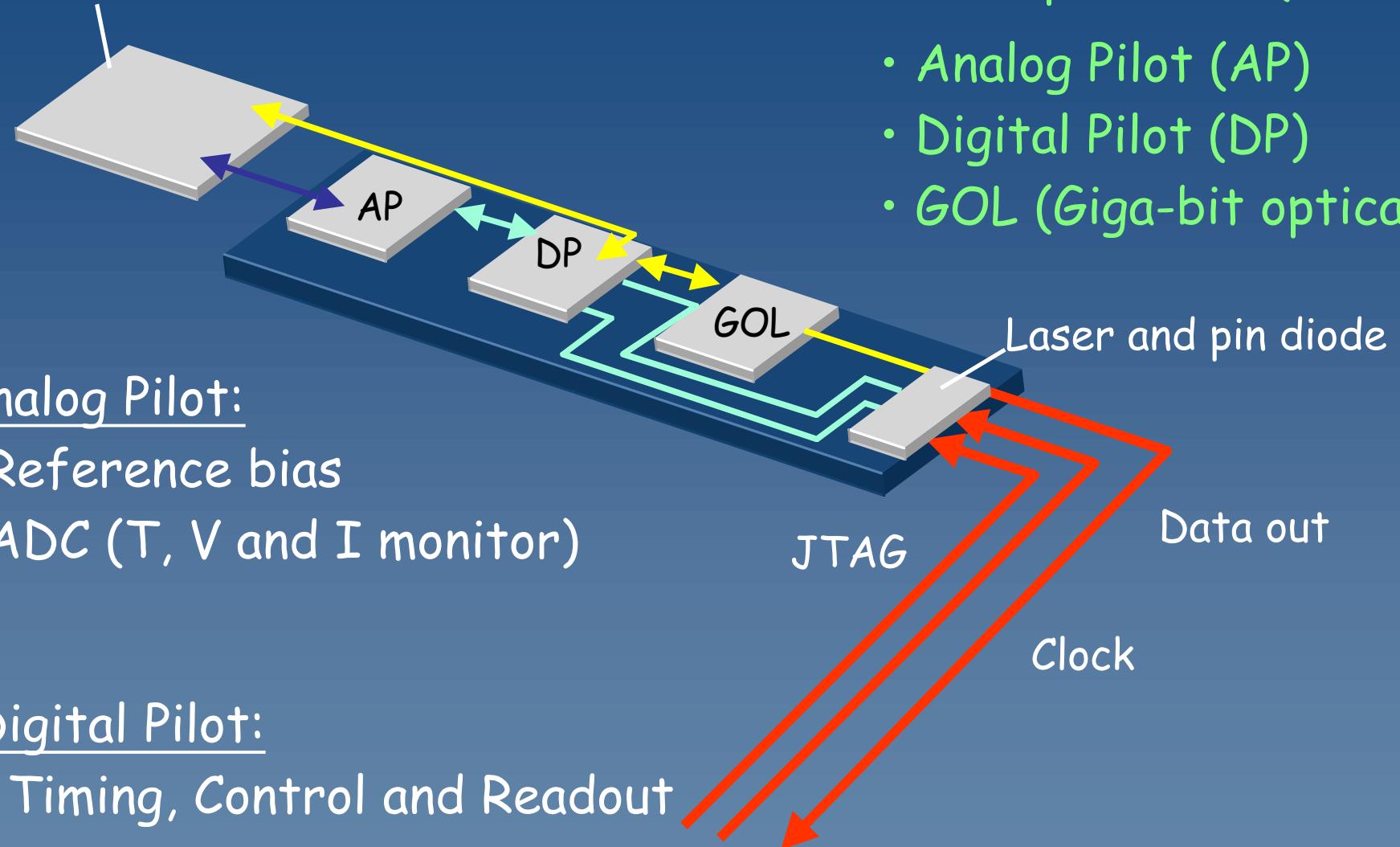
193 mm long

Bus:

- 7 layer Al-Kapton flex
- Wire bonds to the ALICE1LHCb chip

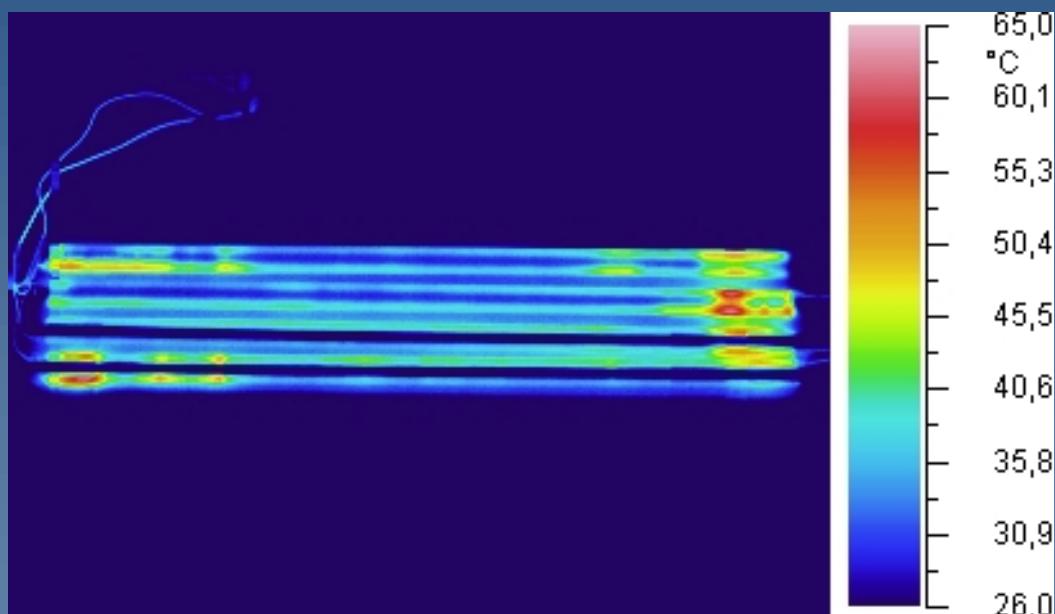


ALICE1LHCb chip



Cooling tests

- ~1.5 kW ($1200 \times 800\text{mW} + \dots$) of dissipated power in the whole SPD
- two phase evaporative cooling system under study



Infrared camera, measurement using resistive network

The ALICE SPD in numbers

- 60 staves
- 240 silicon sensors
- 1200 readout chips
- 240 ladders
- Bump bonds: 9.83 millions
- Wire bonds: ~150.000

SPD Collaboration

Universita e Sezione INFN Bari, Italy

Universita e Sezione INFN Catania, Italy

CERN, Geneva, Switzerland

Slovak Academy of Sciences Kosice, Slovakia

Laboratori Nazionali di Legnaro, Italy

Universita e Sezione INFN Padova, Italy

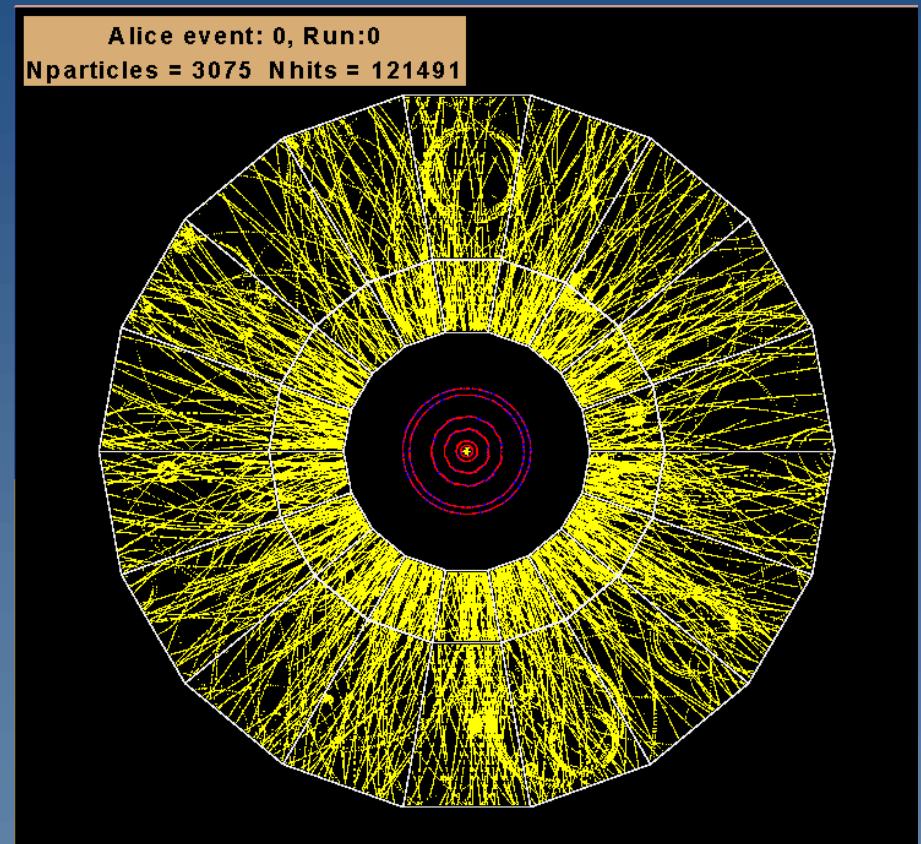
Universita e Sezione INFN Rome, Italy

Universita e Sezione INFN Salerno, Italy

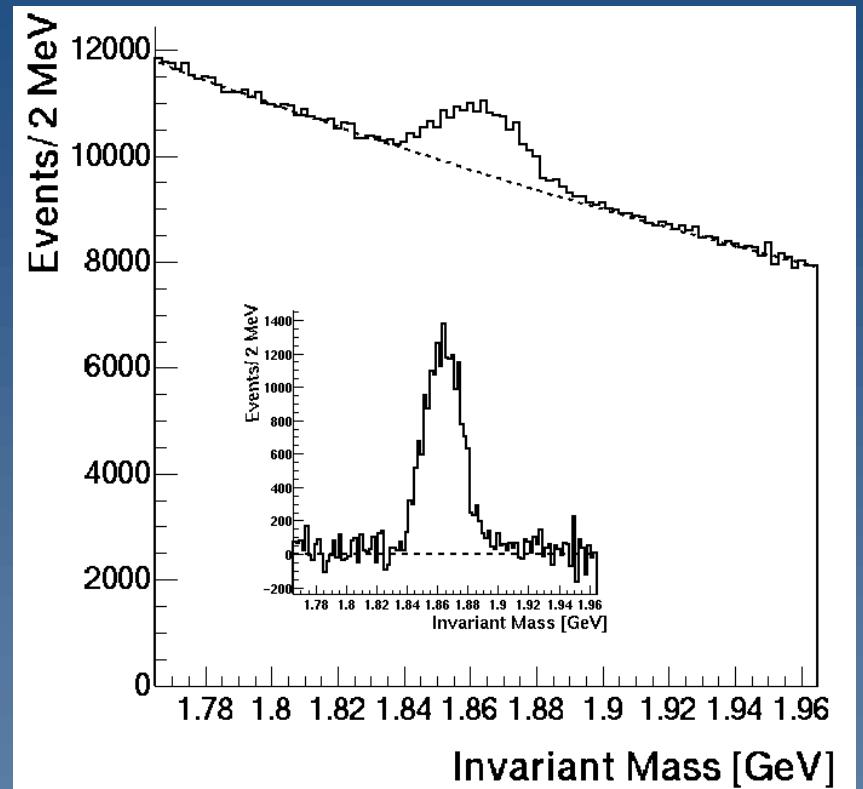
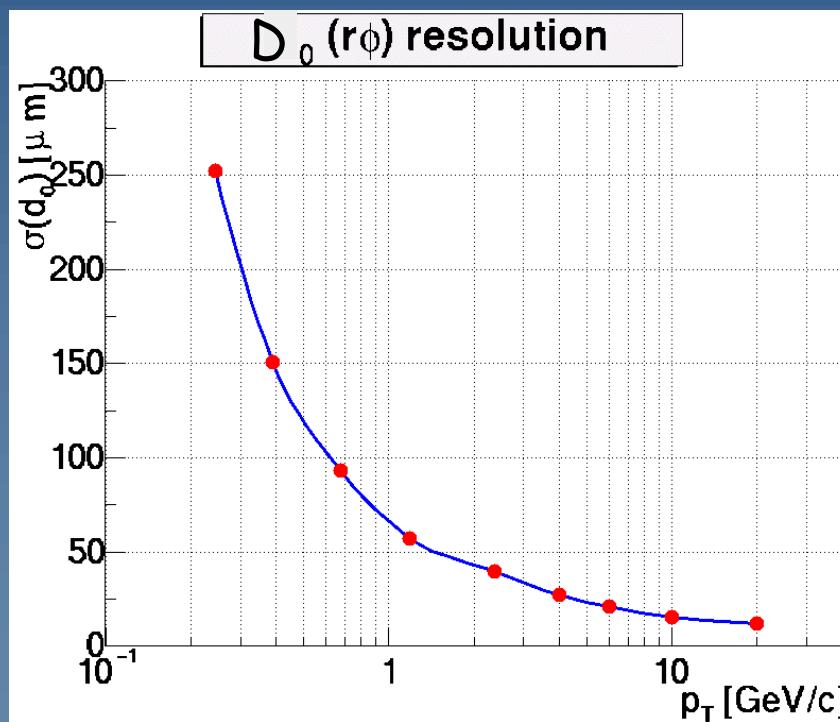
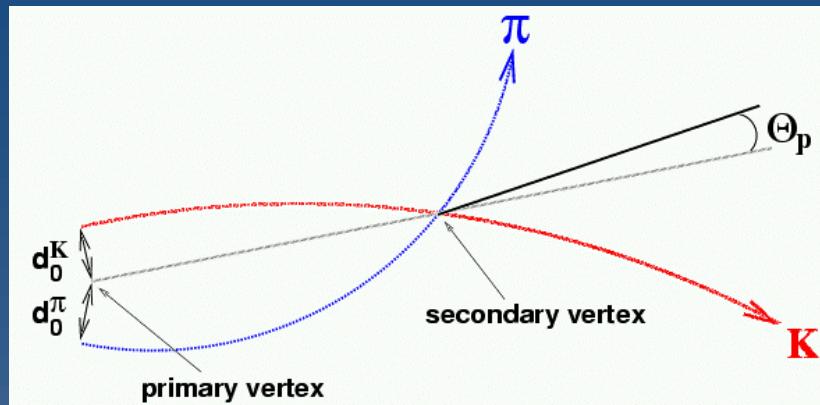
Universita e Sezione INFN Udine, Italy

Physics Performance

- Secondary vertexing capability for charm and beauty detection
- Charged particle multiplicities of up to 8000 per unit of rapidity have been predicted for head-on Pb-Pb collisions at the LHC
- Pseudorapidity coverage of the inner layer: $|\eta| < 1.95$
- The two SPD layers allow to achieve a track impact parameter resolution in the $r\phi$ coordinate better than $50 \mu\text{m}$ for $p_t > 1.3 \text{ GeV}/c$.



A. Dainese - QM2002

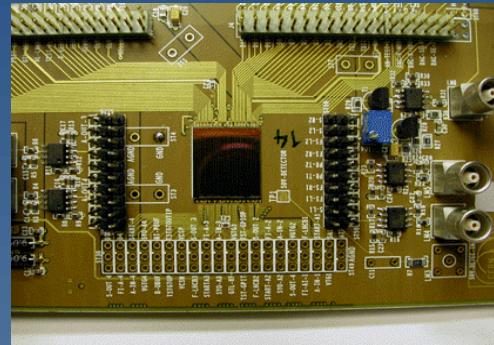


$D^0 \rightarrow K^- \pi^+$ 15 days Pb-Pb data taking
significance (S/\sqrt{B}) = 35

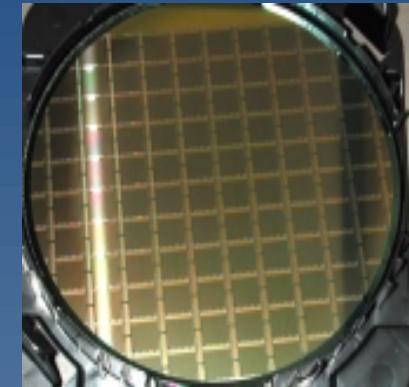
Test System

A modular test system based on VME and LabView was developed in order to test:

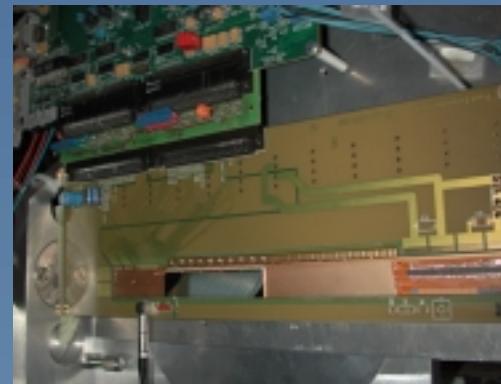
- single chips
- chip wafers
- single assemblies
- ladders
- a full half-stave
- and for the test beam



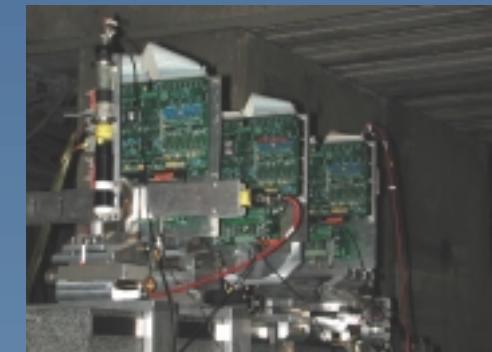
Single chip mounted on card



Chip wafer

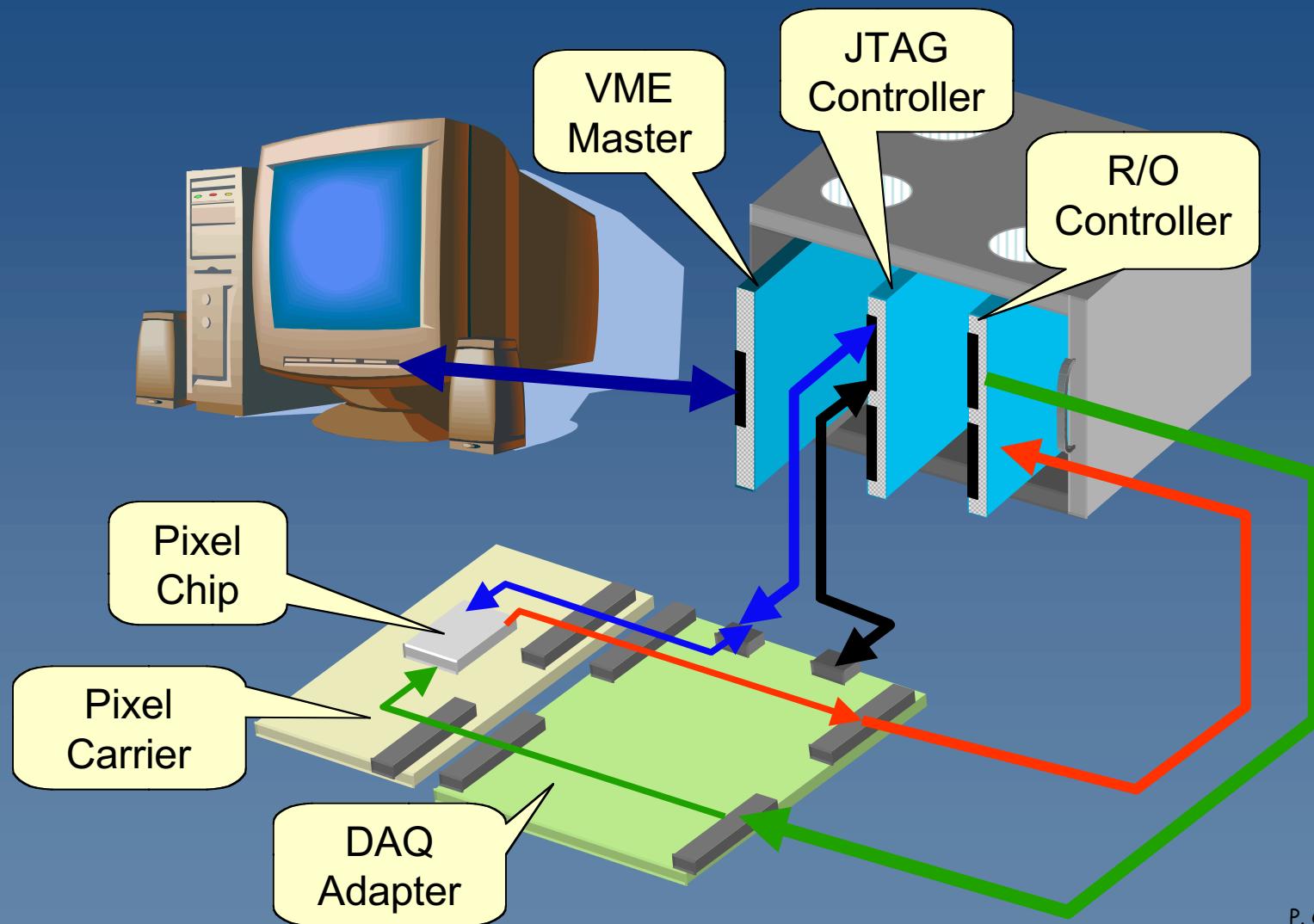


Ladder



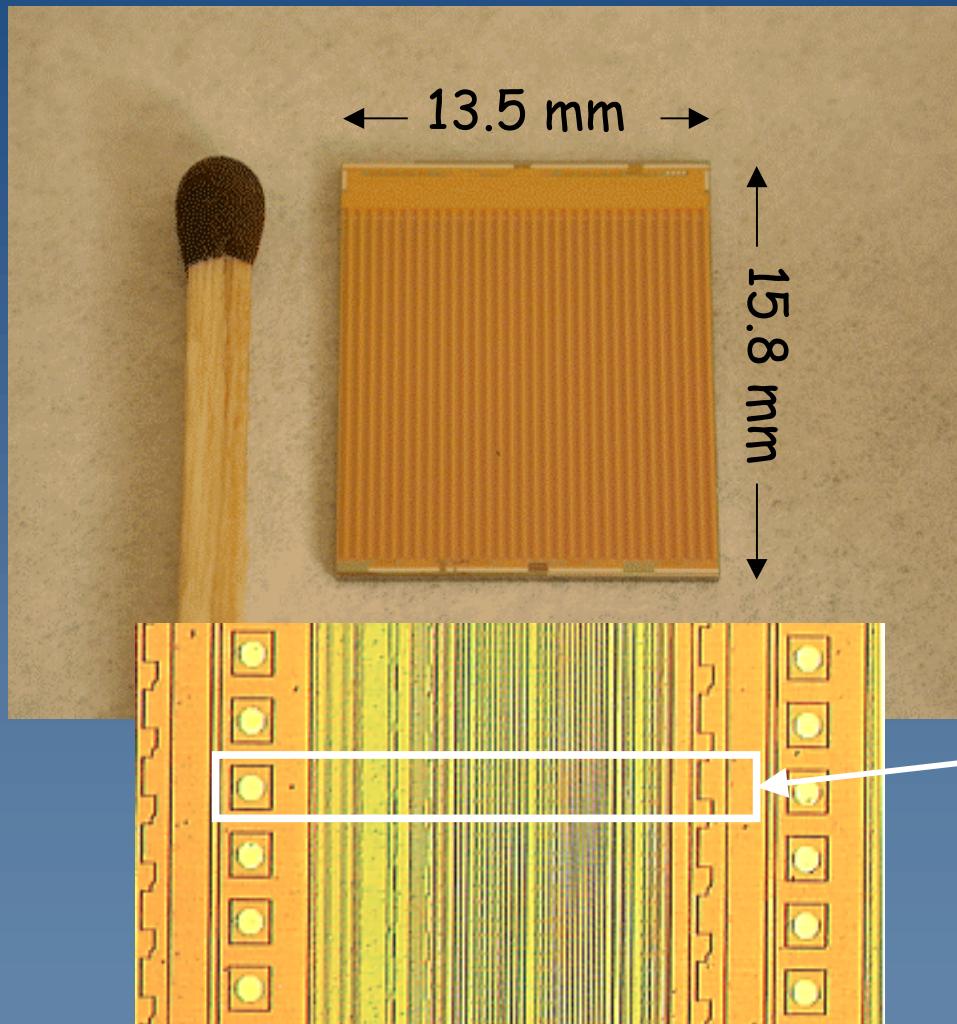
Test beam setup

Test System



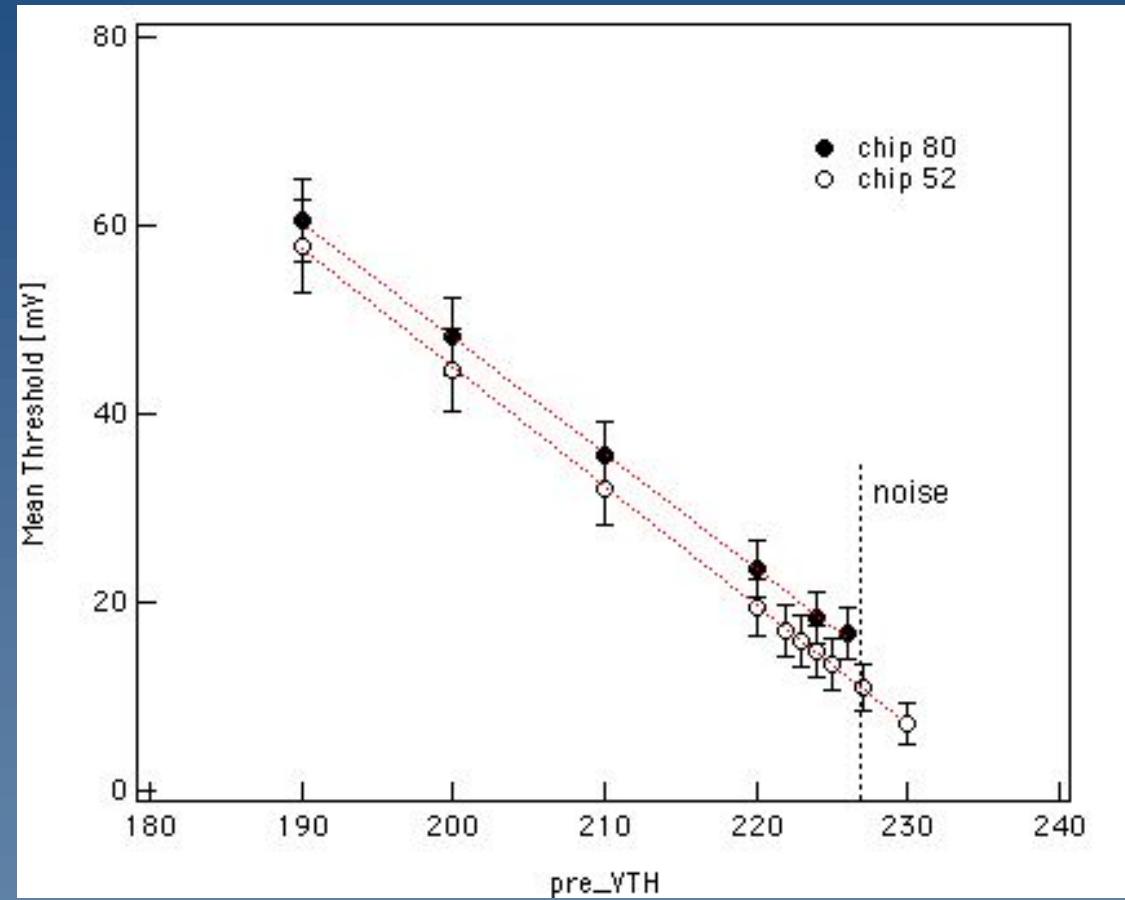
P. Chochula

ALICE1LHCb chip



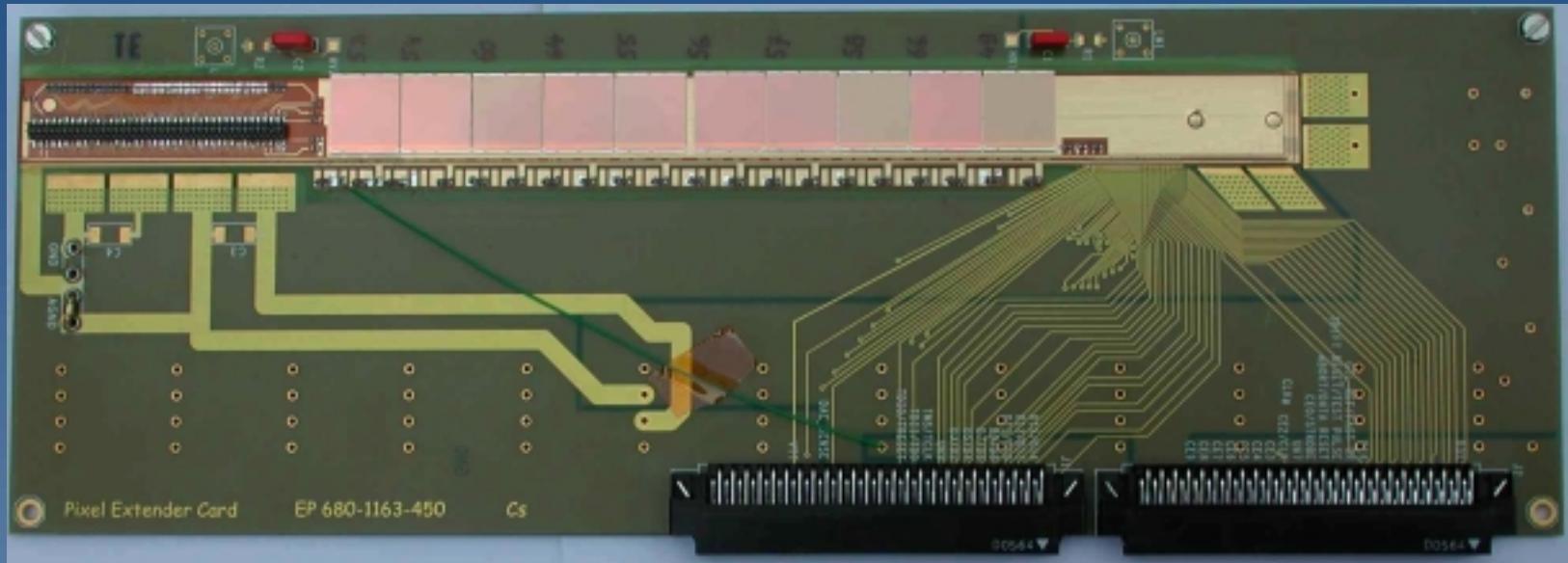
- Mixed signal (analogue, digital)
- Produced in a commercial $0.25\mu\text{m}$ CMOS process
- Radiation tolerant design (enclosed gates, guard rings)
- 8192 pixel cells
- $50\ \mu\text{m} \times 425\ \mu\text{m}$ pixel cell
- $\sim 100\ \mu\text{W}/\text{channel}$

Measurements carried out on one single chip and on one bump-bonded assembly using the test pulse



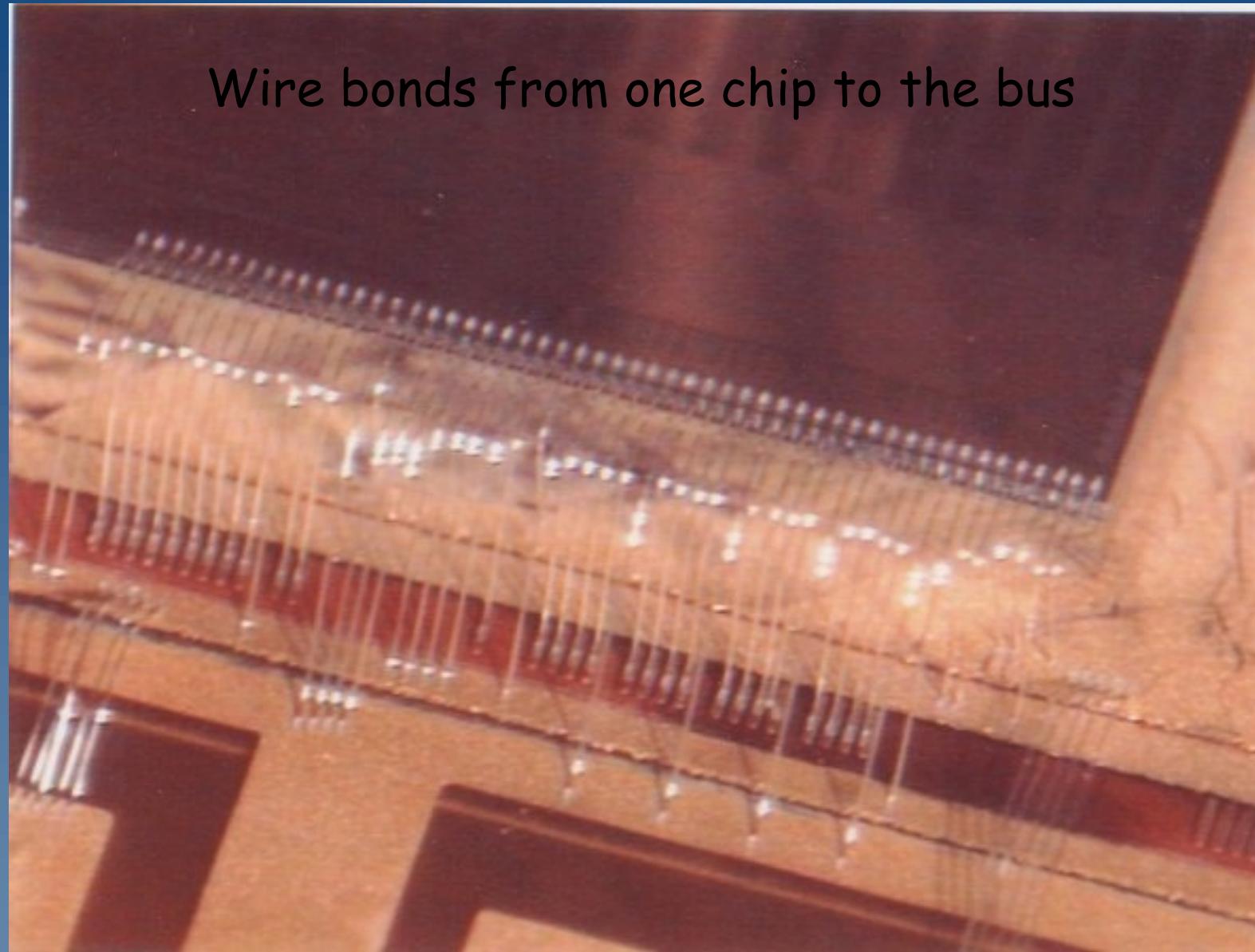
Low minimum threshold: ~1000 electrons
Low individual pixel noise:~100 electrons

First Bus Prototype (Cu-Kapton Flex)



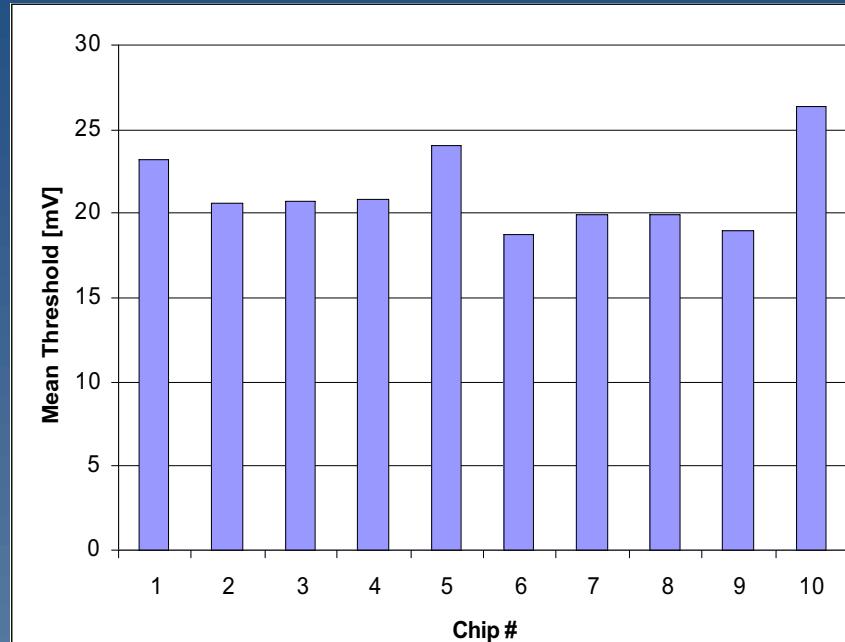
10 chips (pre-tested) mounted

Wire bonds from one chip to the bus



M. Morel

Tests carried out on a bus equipped with 10 ALICE1LHCb chips



Mean Threshold

Tests of voltage sensitivity, sensitivity to clock signal and threshold measurements successfully passed.

Wafer probing

- Tests have been developed gradually during last year
- Completed test procedure for production since spring 2002:
Current consumption, DACs, JTAG, min. threshold, threshold-scan

Introduced 3 chip classes:

1. Chips for bump bonding

mean th<30mV, <1% defect pixels, $I_{\text{analog}} < 350\text{mA}$, $I_{\text{digital}} < 270\text{mA}$

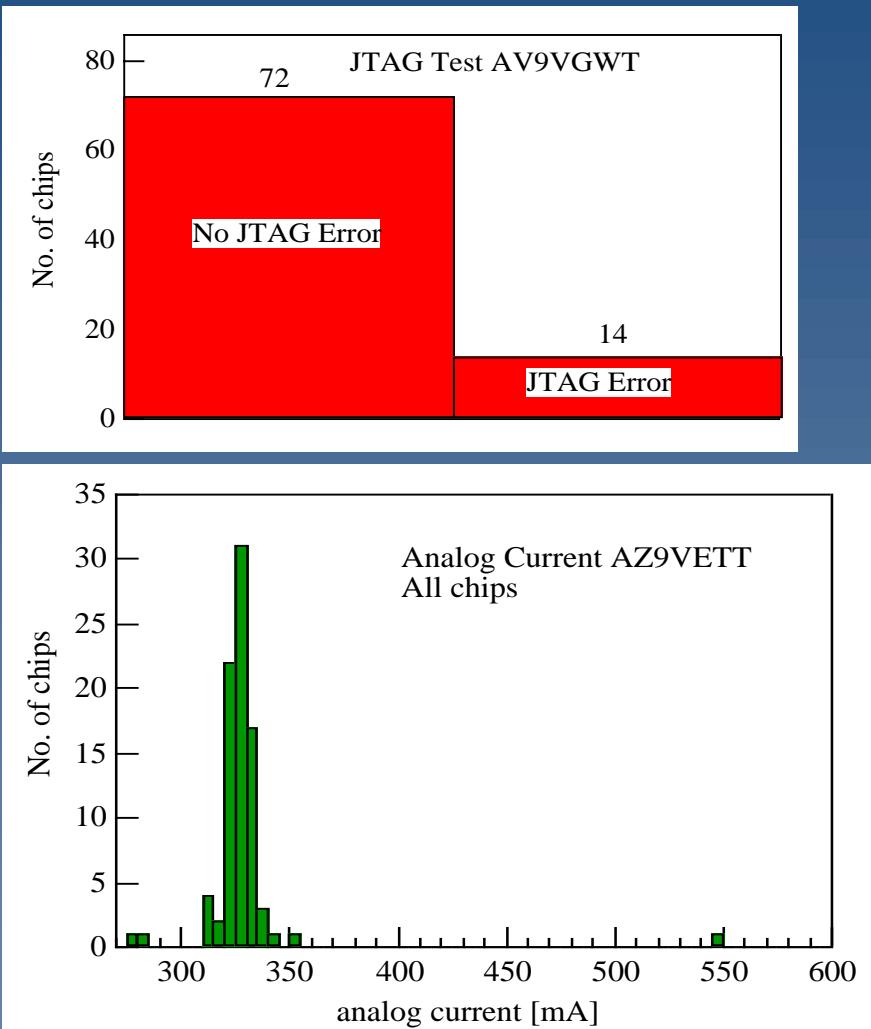
2. Minor defects

missing columns, >1% defect pixels

3. Major defects

JTAG error (10-20%), DAC error, no/high current, digital out error

86 ALICE1LHCb chips per 200mm wafer



Example Class III:

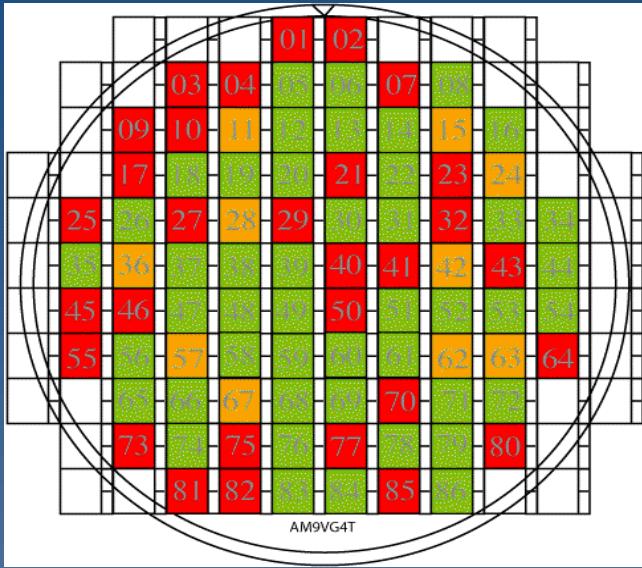
JTAG test on one wafer:
14 chips with errors

Crucial test: serial connection of
all chips on a half-stave

Example Class I:

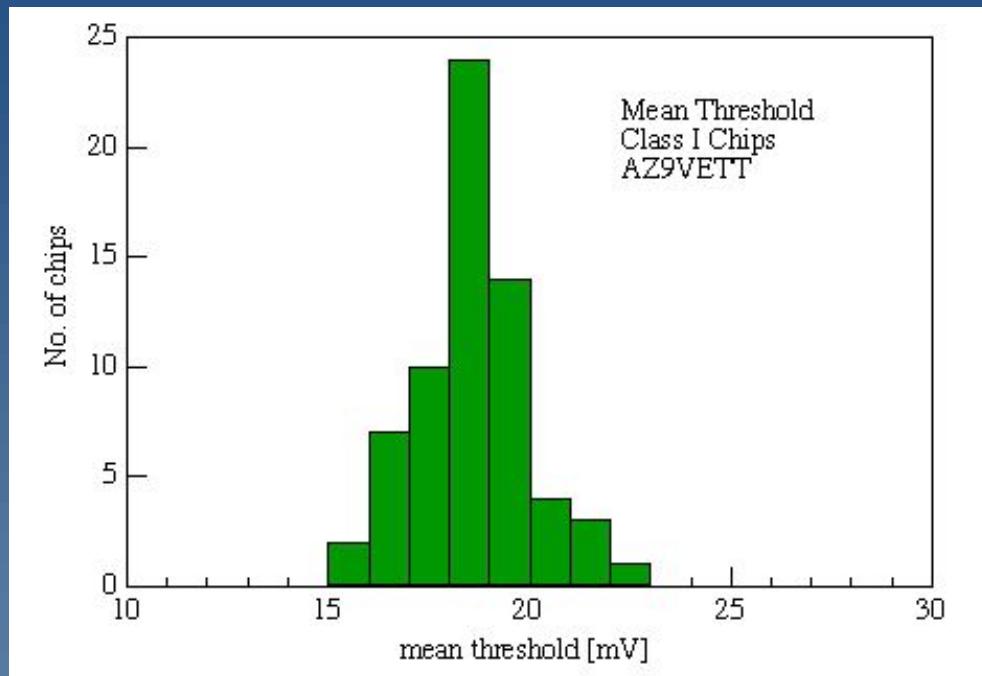
$I_{\text{digital}} < 270\text{mA}$: no working chip
exceeds this value

$I_{\text{analog}} < 350\text{mA}$: loose 15 working chips
due to this cut out of 344 chips



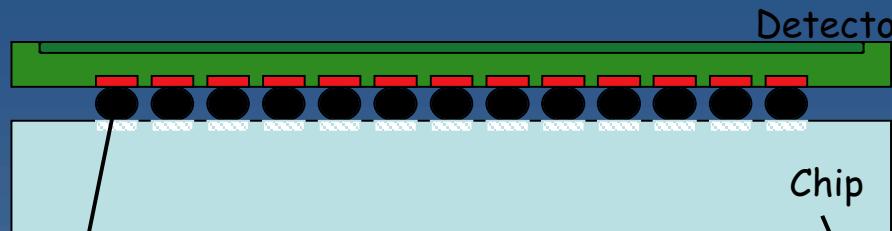
Class I: 42-75%
 Class II: 6-12%
 Class III: 17-42%
 (sample: 4 wafer, 750µm)

Class I - Mean Threshold



Production testing will start this autumn

Ladders and Assemblies



Bump-bonding:

- VTT/Finland
Pb-Sn solder bumps
- AMS/Italy
In bumps

Detectors:

- single chip detectors
- 5 chip detectors for ladders
- p-in-n
- $300 \mu\text{m}$ thick(tests) - final thickness: $200\mu\text{m}$

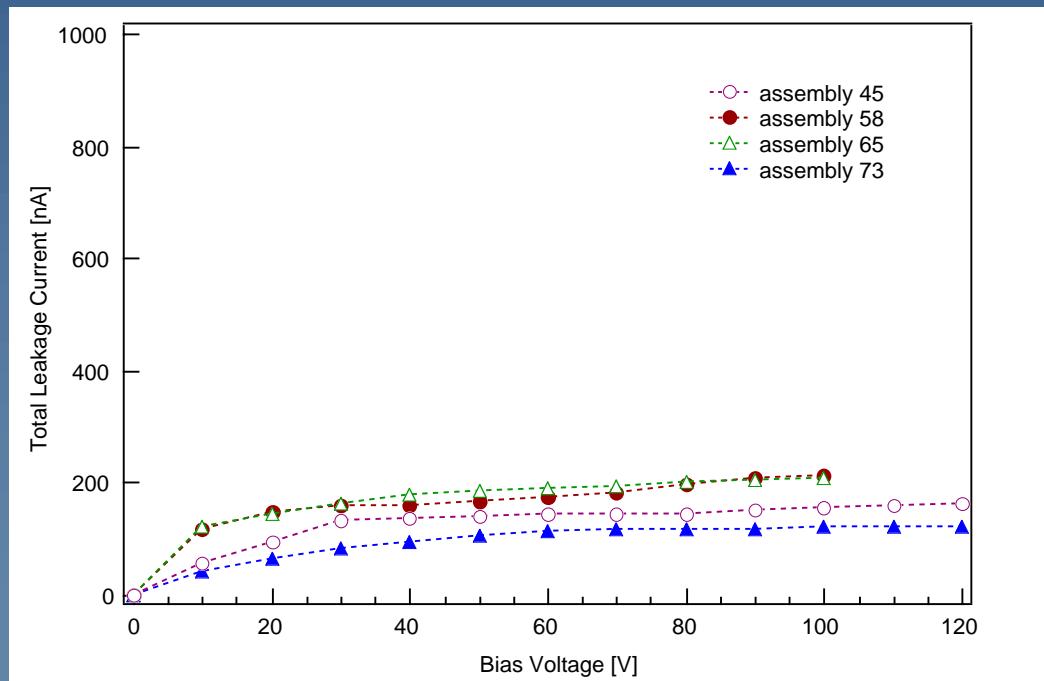
Chips:

- single chips
- $750 \mu\text{m}$ thick (tests) - $150\mu\text{m}$ final

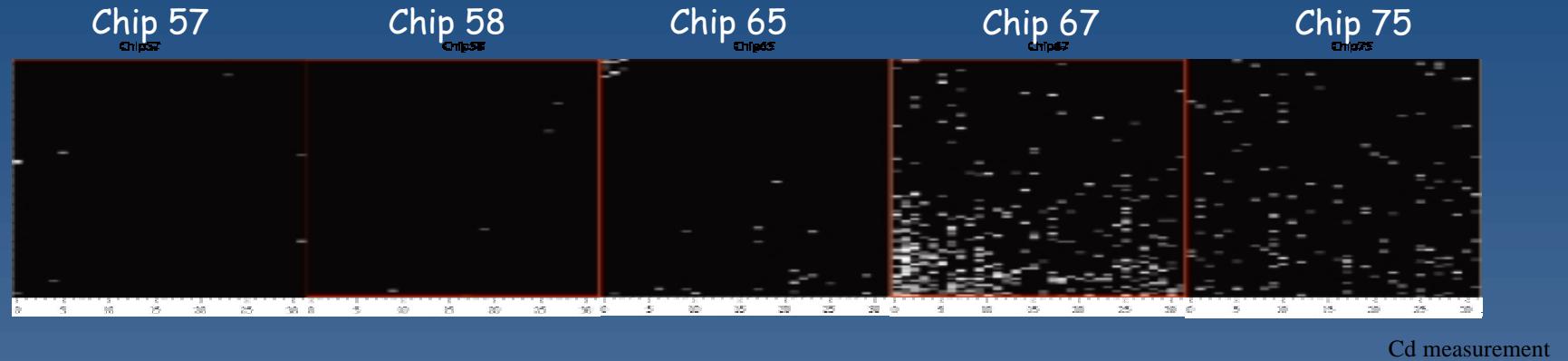
Detectors

- P-in-n detectors with simple guard ring structure
- Calculated fluence in ALICE: $\sim 10^{12}$ (1 MeV n/cm²) in layer1 in 10 years
- Depletion voltage: 300 μ m test detectors: 21V, 200 μ m test detectors: 12V
- Production starting Winter 2002

Total Leakage Current vs. Bias Voltage



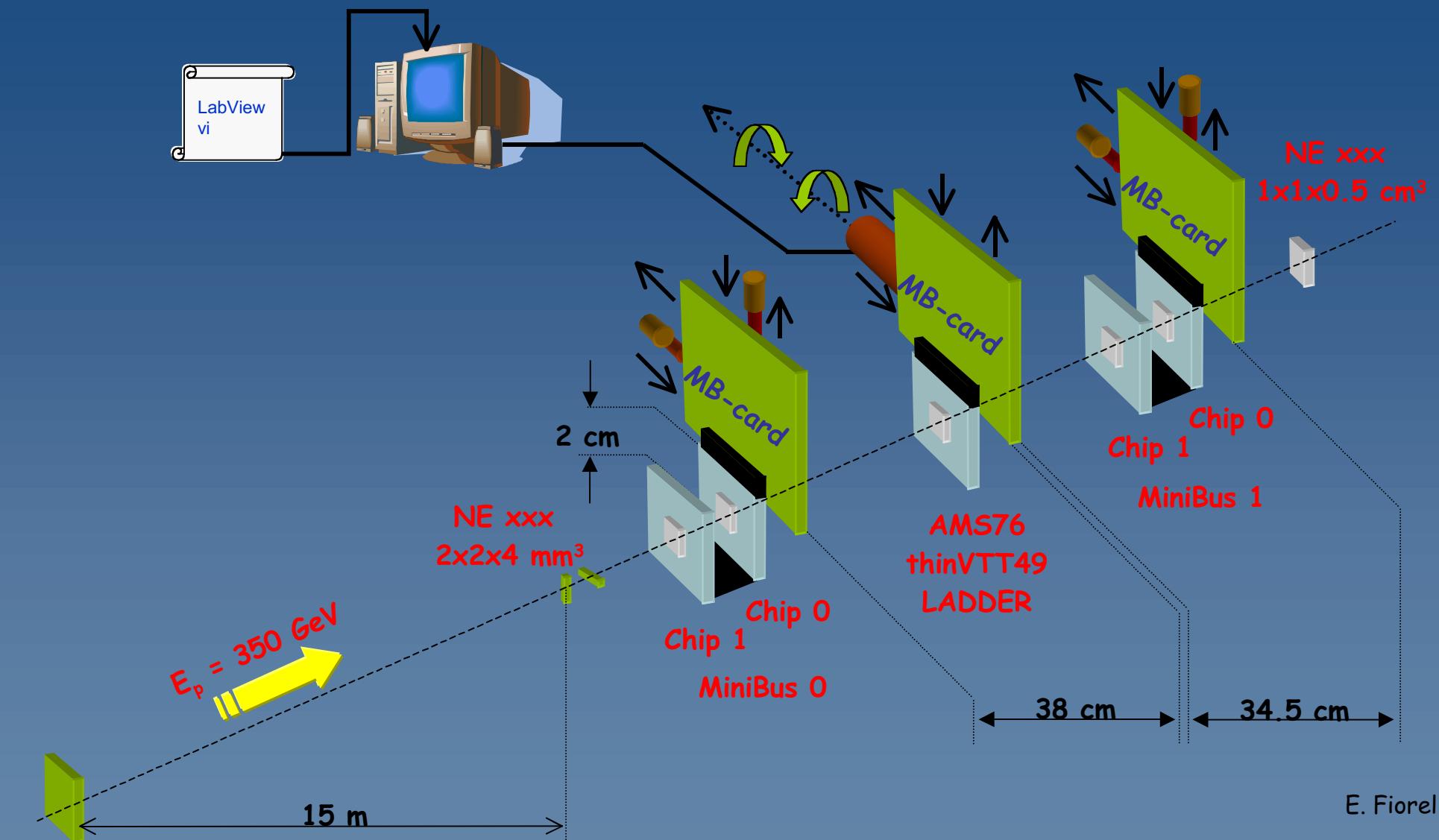
VTT Ladder2:
Detector: $3.1\mu\text{A}$ @ 80V



Pixels with hits:

chip	Sr	Cd	
75	98.5 %	97.9 %	3 noisy pixel
67	94.1 %	94.2 %	2 noisy pixel
65	99.4 %	99.2 %	
58	99.5 %	99.5 %	
57	99.4%	99.5 %	1 noisy column

Test beam 2002

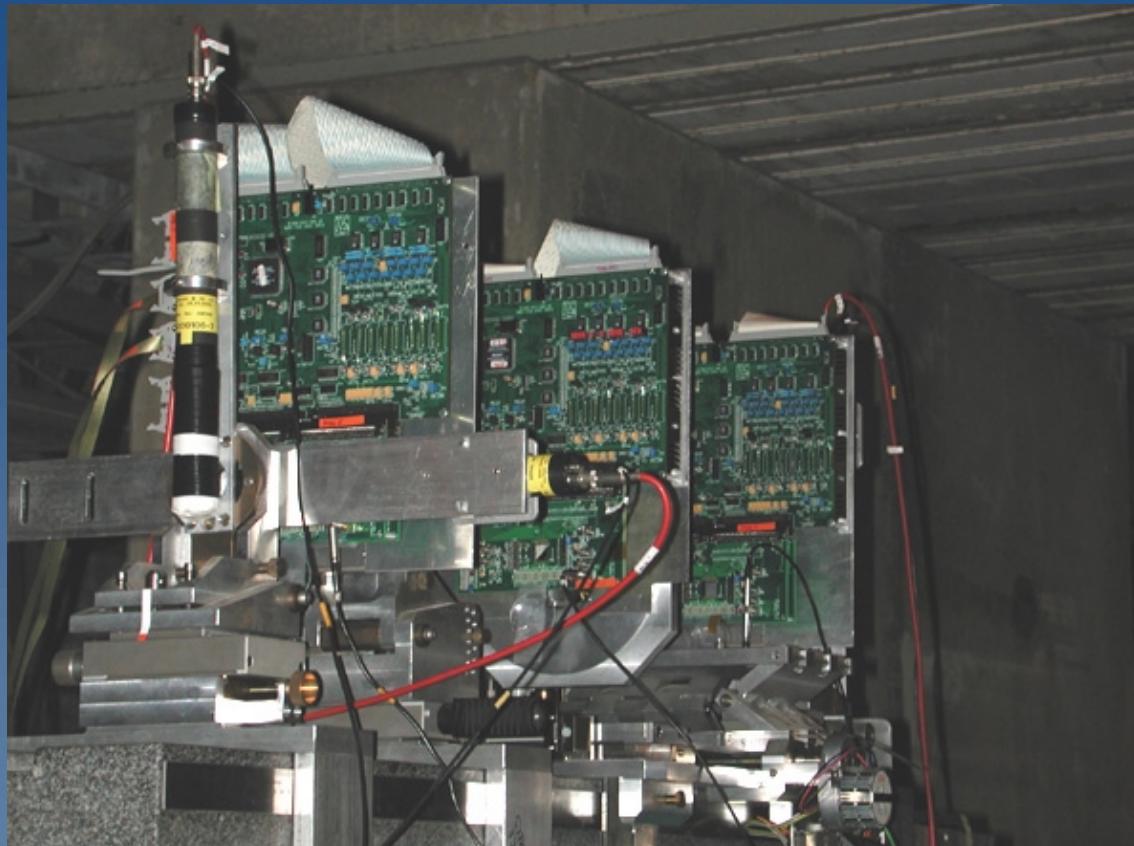


$\text{NE } \text{xxx}$
 $5 \times 5 \times 0.5 \text{ cm}^3$
PIXEL 2002 - 9/9/2002

P. Riedler/CERN

E. Fiorello

27



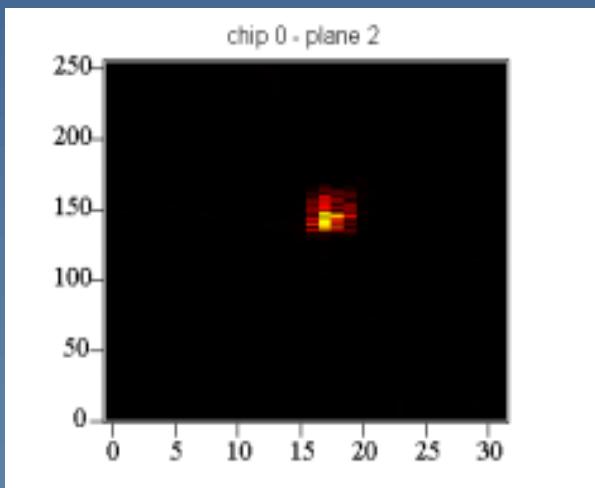
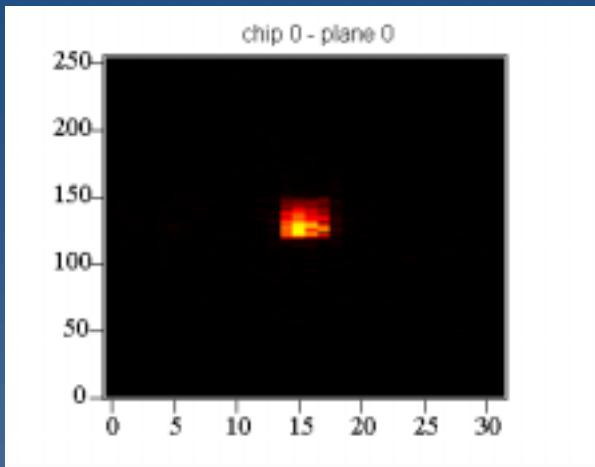
July 3-17, 2002
H4 test beam area, CERN

Trigger: 4 scintillators
2mm x 2mm beam spot

Reference planes:
2 mini-buses (4 pixel assemblies)
with 16384 pixels each

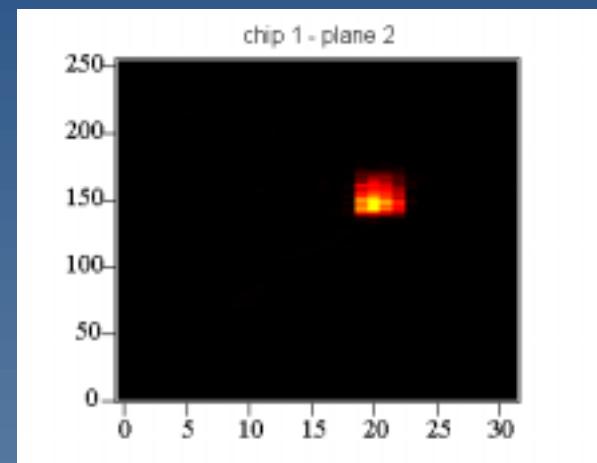
Tested:
1 thick assembly
1 thin assembly ($200\mu\text{m}$ det.)
1 full ladder

Beam spot



Plane 0

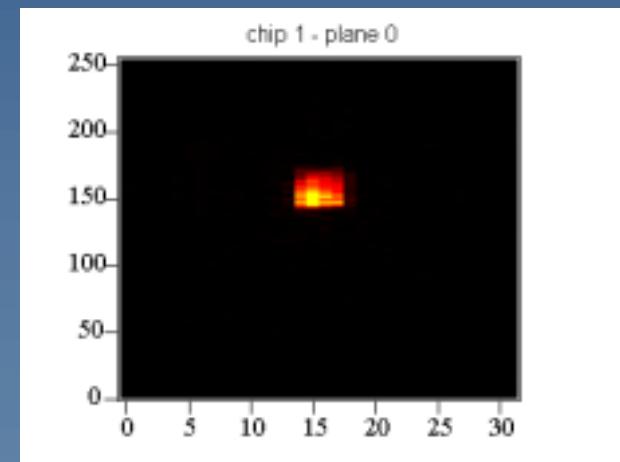
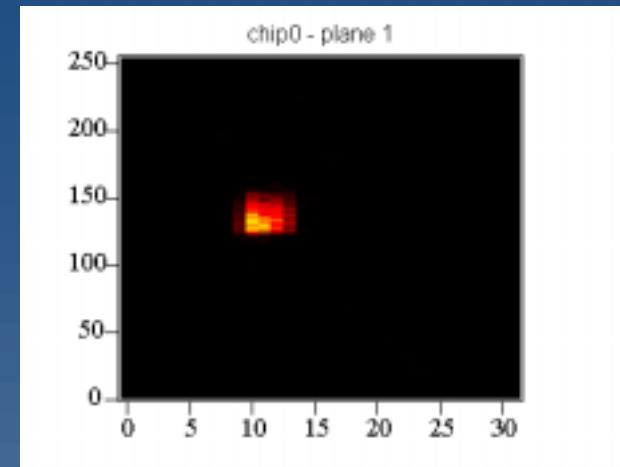
PIXEL 2002 - 9/9/2002



AMS 76

Plane 1

P. Riedler/CERN

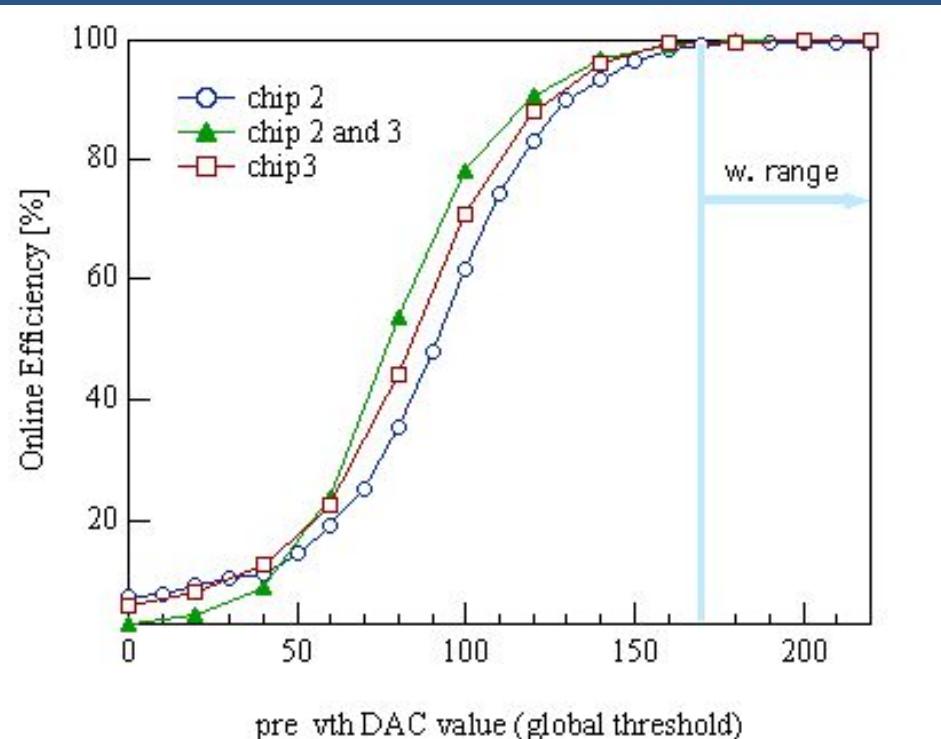


Plane 2

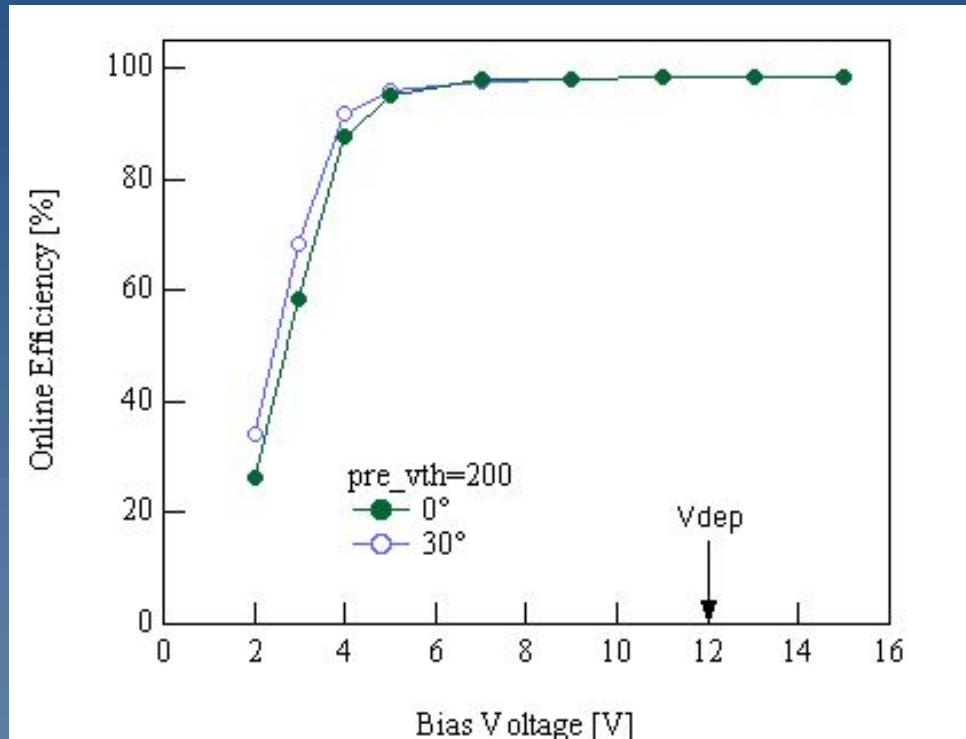
29

Online Measurements

Ladder



Thin assembly

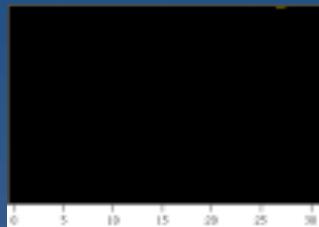


Threshold-scan

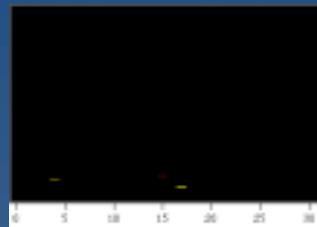
Bias Scan

Beam spot on VTT-ladder

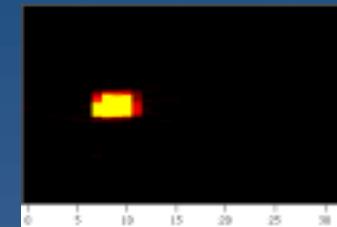
chip0



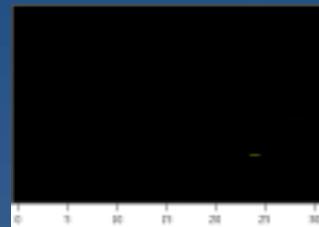
chip1



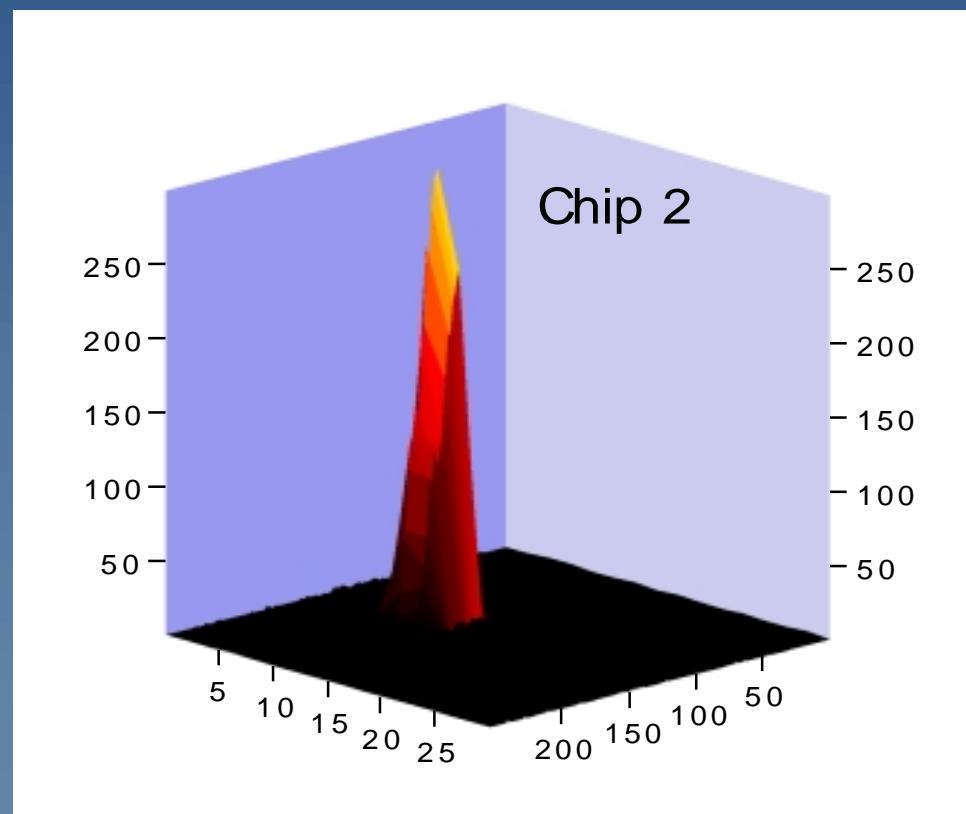
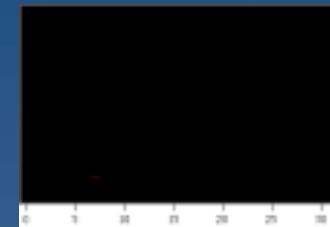
chip2



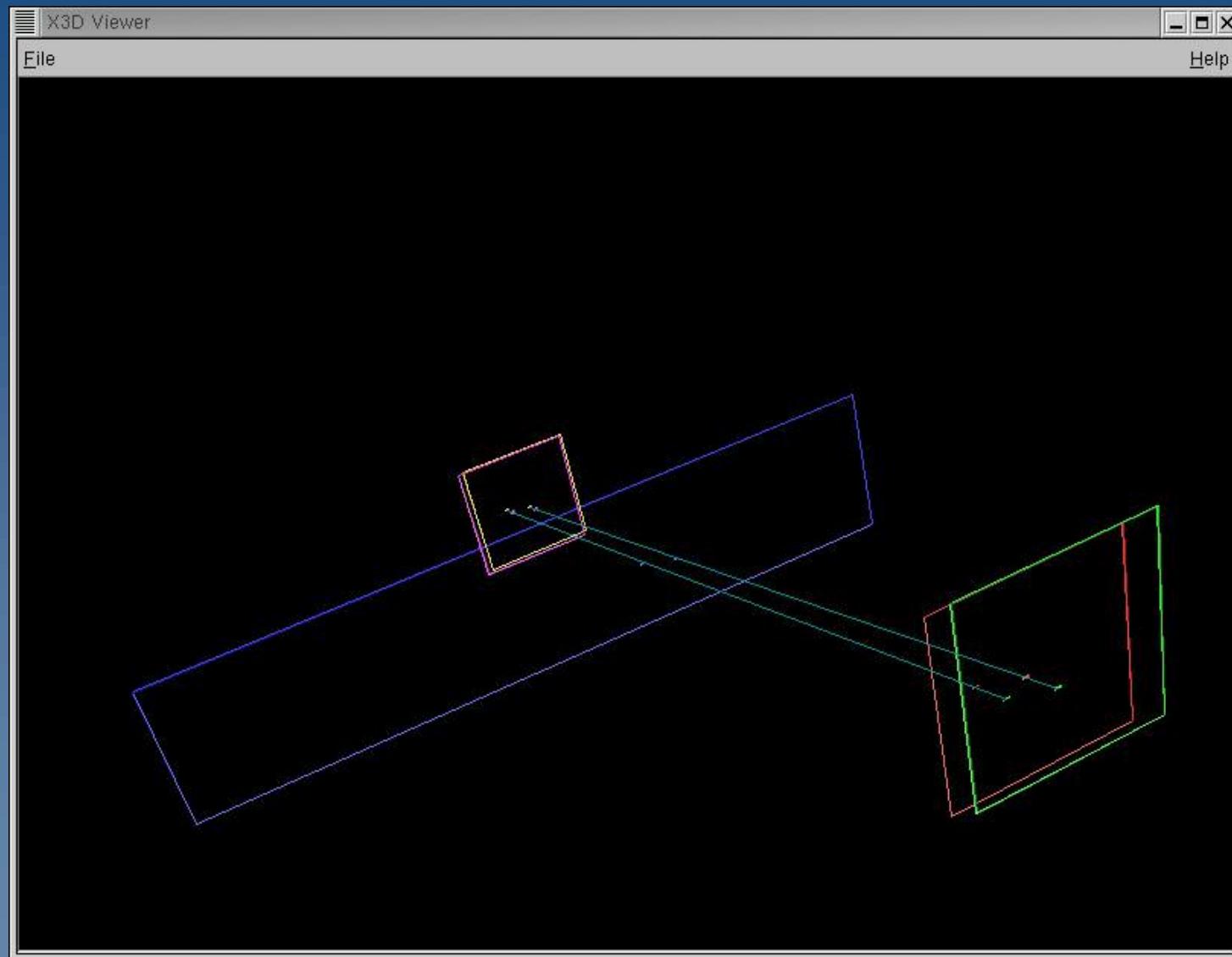
chip3

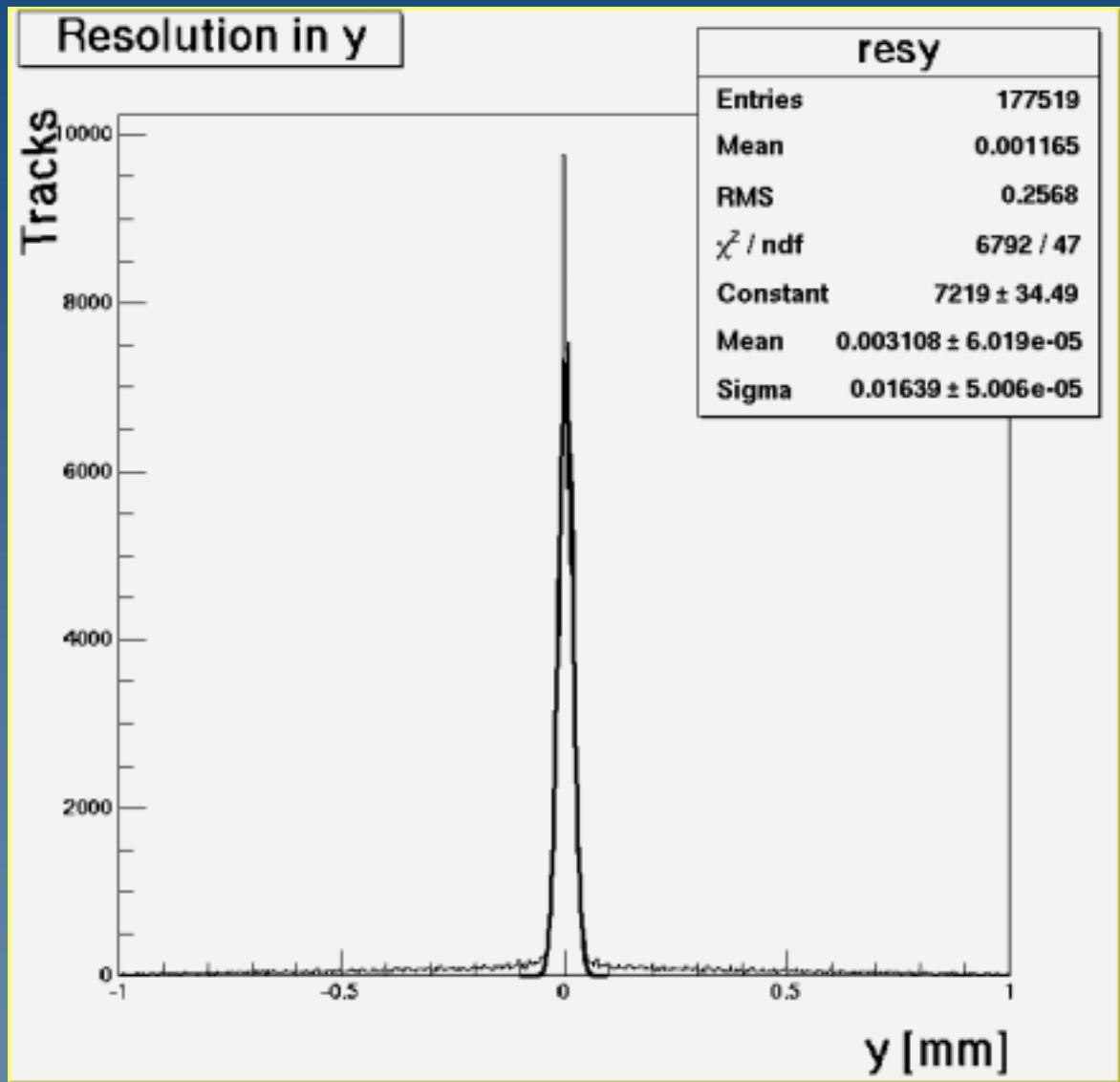


chip4



Reconstructed tracks in the ladder using the Mini-buses





Residual - Preliminary!

50 μm 425 μm

measured along the
50 μm axis: $\sigma_y = 16.4\mu\text{m}$

Pitch/sqrt(12)=14.4 μm

Conclusions and Summary

- The ALICE1LHCb chip has been qualified for ALICE.
- A wafer testing procedure has been established.
- A 10-chip bus has been tested successfully in the lab.
- A full size ladder has been tested successfully in a test beam.

Next Steps:

- The complex assembly procedure is in preparation.
- 8" wafer thinning and assembly.
- Building a complete half stave is foreseen for 2003.
- System integration issues are under study.